S/N 09/551,027 **PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**



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| Applicant: | Wendell P. Noble et al. | Examiner: Michael Trinh |
| Serial No.: | 09/551,027 | Group Art Unit: 2822 |
| Filed: | April 17, 2000 | Docket: 303.379US2 |
| Title: | CIRCUIT AND METHOD FOR A FOLDED BIT LINE MEMORY CELL WITH VERTICAL TRANSISTOR AND TRENCH CAPACITOR | |

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## INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants further request that a copy of the 1449 form, initialled by the Examiner to indicate that all listed citations have been considered, be returned with the next official communication.

Under 37 C.F.R. §1.97(b)(3), it is believed that no fee or certificate is required with this Information Disclosure Statement.

The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.



Respectfully submitted,

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By their Representatives,

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"Express Mail" mailing label number: EL721276345US
Date of Deposit: September 19, 2001
This paper or fee is being deposited on the date indicated above with the United States Postal Service pursuant to 37 CFR 1.10, and is addressed to the Commissioner for Patents, Box CPA, Washington, D.C. 20231.